Amendments to the Claims:

Please cancel Claim 3 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure, comprising:

forming a gate structure on a surface of a semiconductor substrate, wherein said gate structure includes a first vertical surface and a second vertical surface;

forming a first spacer adjacent to said first vertical surface and a second spacer adjacent to said second vertical surface, wherein said first spacer has a first thickness and a second thickness that is greater than said first thickness and that abuts said first vertical surface, and wherein said second spacer has a third thickness and a fourth thickness that is greater than said third thickness and that abuts said second vertical surface, wherein said step of forming said first and second spacers comprises:

depositing a first mask on said surface and said gate structure;

depositing a second mask on said surface and said gate structure;

performing a first plasma etch process to remove substantially said second mask;

performing a second plasma etch process to remove substantially said first mask; and

performing a third plasma etch process to remove completely said second mask such that a remaining portion of said first mask defines said first and second spacers; and

performing a single implant process to form said triple LDD structure for a drain and a source of said semiconductor device in said semiconductor substrate.

2. (Original) The method as recited in Claim 1 further comprising:

performing a silicidation process such that a silicide is formed on a horizontal surface of said gate structure, a first upper portion of said first vertical surface, and a second upper portion of said second vertical surface.

3. (Cancelled)

4. (Currently Amended) The method as recited in Claim 1 [[3]] wherein said first plasma etch process uses a first plasma that has a first etch rate with respect to said first mask and a second etch rate with respect to said second

mask, and wherein said second etch rate is substantially greater than said first etch rate.

5. (Currently Amended) The method as recited in Claim 1 [[3]] wherein said second plasma etch process uses a second plasma that has a first etch rate with respect to said first mask, a second etch rate with respect to said second mask, and a third etch rate with respect to said gate structure, and wherein said first etch rate is substantially greater than said second etch rate and said third etch rate.

6. (Currently Amended) The method as recited in Claim 1 [[3]] wherein said third plasma etch process uses a third plasma that has a first etch rate with respect to said first mask, a second etch rate with respect to said second mask, and a third etch rate with respect to said gate structure, and wherein said second etch rate is substantially greater than said first etch rate and said third etch rate.

7. (Currently Amended) The method as recited in Claim 1 [[3]] wherein said first mask is silicon nitride.

8. (Currently Amended) The method as recited in Claim 1 [[3]] wherein said second mask is silicon dioxide.

9. (Previously Presented) The method as recited in Claim 1 wherein said single implant process is an ion implant process.

10. (Original) The method as recited in Claim 1 wherein said semiconductor device is a MOSFET (metal oxide semiconductor field effect transistor).

11. (Original) A method of fabricating a semiconductor device having a triple LDD (lateral diffused dopants) structure, comprising:

forming a gate structure on a surface of a semiconductor substrate, wherein said gate structure includes a first vertical surface and a second vertical surface;

depositing a first mask on said surface and said gate structure;

depositing a second mask on said surface and said gate structure;

performing a first plasma etch process to remove substantially said second mask;

performing a second plasma etch process to remove substantially said first mask;

performing a third plasma etch process to remove completely said second mask such that a remaining portion of said first mask defines a first spacer adjacent to said first vertical surface and a second spacer adjacent to said

second vertical surface, wherein said first spacer has a first thickness and a second thickness that is greater than said first thickness and that abuts said first vertical surface, and wherein said second spacer has a third thickness and a fourth thickness that is greater than said third thickness and that abuts said second vertical surface; and

performing an implant process to form said triple LDD structure for a drain and a source of said semiconductor device in said semiconductor substrate.

12. (Original) The method as recited in Claim 11 further comprising:

performing a silicidation process such that a silicide is formed on a horizontal surface of said gate structure, a first upper portion of said first vertical surface, and a second upper portion of said second vertical surface.

13. (Original) The method as recited in Claim 11 wherein said first plasma etch process uses a first plasma that has a first etch rate with respect to said first mask and a second etch rate with respect to said second mask, and wherein said second etch rate is substantially greater than said first etch rate.

14. (Original) The method as recited in Claim 11 wherein said second plasma etch process uses a second plasma that has a first etch rate with respect to said first mask, a second etch rate with respect to said second mask, and a

third etch rate with respect to said gate structure, and wherein said first etch rate is substantially greater than said second etch rate and said third etch rate.

15. (Original) The method as recited in Claim 11 wherein said third plasma etch process uses a third plasma that has a first etch rate with respect to said first mask, a second etch rate with respect to said second mask, and a third etch rate with respect to said gate structure, and wherein said second etch rate is substantially greater than said first etch rate and said third etch rate.

16. (Original) The method as recited in Claim 11 wherein said first mask is silicon nitride.

17. (Original) The method as recited in Claim 11 wherein said second mask is silicon dioxide.

18. (Original) The method as recited in Claim 11 wherein said implant process is an ion implant process.

19. (Original) The method as recited in Claim 11 wherein said semiconductor device is a MOSFET (metal oxide semiconductor field effect transistor).

20. (Withdrawn) A semiconductor device comprising:

a drain having a triple LDD (lateral diffused dopants) structure;

a source having a triple LDD (lateral diffused dopants) structure;

a gate structure including a first vertical surface, a second vertical surface, and a horizontal surface; and

a silicide formed on said horizontal surface, a first upper portion of said first vertical surface, and a second upper portion of said second vertical surface.

21. (Withdrawn) The semiconductor device as recited in Claim 20 wherein said semiconductor device is a MOSFET (metal oxide semiconductor field effect transistor).